Such LUT for the input variables logic functions is the use of LUT in four variables (4-LUT). The OUT output. Variable inverters ensure the realization of all members of a PDNF. The speed of computing logic functions determines by the delay in the coupling matrices, so this decomposition leads to a decrease in performance. In recent years, the direction of adaptive logic modules (ALM) has been actively developing, in which the user has access to various versions of logical elements for five, six and even seven, eight variables, which leads to an increase in performance. However, the manufacturer’s documentation does not provide a detailed description of the features of such multi-input LUTs, taking into account the Meade-Conway constraints. In addition, there are no estimates of complexity and speed of multi-input LUTs. The analysis of sources allows suggests a further increase in the LUT bit capacity and the convergence of FPGA and CPLD (complex programmable logic devices) capabilities in terms of bit depth. Therefore, studies of the features of constructing multi-input LUTs are relevant and the authors attempted to analyze the implementation of such prospective multi-bit logic modules.

Objective. The purpose of this work is to estimate the complexity and speed of the decomposition of a multi-bit LUT.

Method. Obtaining expressions for estimating the complexity and speed of decomposition of a multi-bit LUT on a LUT of a lower bit length.

Results. A comparison of the complexity and delay in the number of transistors in the decomposition of a multi-bit LUT in the computer mathematics system Mathcad is performed.

Conclusions. The conducted researches made it possible to establish the features of constructing multi-bit LUTs and to evaluate various variants of decomposition with further increase in the LUT dimension with the subsequent choice of the optimal ALM variant.

Keywords: logic element, FPGA, LUT, transistor, adaptive logic module, decomposition, complexity, speed.

STUDY OF THE MULTI-INPUT LUT COMPLEXITY

Contex. The programmable logic integrated circuits FPGA (field-programmable gate array) used realization of the generator of functions LUT (Look Up Table), which is configured by loading a configuration memory for calculating a logic function in perfect disjunctive normal form (PDNF). The LUT dimension determines the technological limitations of Mead and Conway on the number of series-connected MOS transistors. The standard number of LUT inputs for many years was 3 or 4, and 4-LUT is constructed from two 3-LUTs with an additional 1-LUT. However, in many projects, it is required to calculate functions of a large number of arguments. This requires a multi-input LUT, which is built as a decomposition of 3-LUT, 4-LUT. The speed of computing logic functions determines by the delay in the coupling matrices, so this decomposition leads to a decrease in performance. In recent years, the direction of adaptive logic modules (ALM) has been actively developing, in which the user has access to various versions of logical elements for five, six and even seven, eight variables, which leads to an increase in performance. However, the manufacturer’s documentation does not provide a detailed description of the features of such multi-input LUTs, taking into account the Meade-Conway constraints. In addition, there are no estimates of complexity and speed of multi-input LUTs. The analysis of sources allows suggests a further increase in the LUT bit capacity and the convergence of FPGA and CPLD (complex programmable logic devices) capabilities in terms of bit depth. Therefore, studies of the features of constructing multi-input LUTs are relevant and the authors attempted to analyze the implementation of such prospective multi-bit logic modules.

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NOMENCLATURE

ALM – adaptive logic module;
FPGA – field programmable gate array;
LAB – physically grouped set of logical resources Logic
Array Block;
LUT – the lookup table;
SRAM – static memory with random access;
LE – logical element;
RAM – random access memory;
ROM – read-only memory;
PDNF – perfect disjunctive normal form;
k – the dimension of the basic LUT;
n – amount of elements;
x_k, x_{k-1} – input variables.

1 PROBLEM STATEMENT

Given: adaptive logic modules FPGA Stratix III in seven variables [4, 5].

In the literature [6–8], the problems of decomposition of multi-bit LUT are not fully covered.

It is required: to assess the complexity and speed of the decomposition of a multi-bit LUT in order to identify features of the construction of adaptive logic modules and the prospects for further increasing the bit capacity.

2 REVIEW OF THE LITERATURE

Stratix III FPGAs have adaptive (ALM) logical blocks that are combined into logical blocks (LAB) [4], which implement functions of even seven variables. The peculiarities of the implementation of such LUTs are of interest. The fact is that due to the limitations of Meade and Conway on the number of consecutively connected transistors [5], the tree of transmitting transistors can not contain more than four transistors in the chain. It is necessary to decompose the multi-bit LUT into LUTs of lesser length, that is, to construct a tree from the subtrees.
FPGA Stratix III is described in a sufficient number of sources [6–8]. The structure of such FPGAs includes the so-called logic array blocks containing ALM, which can be configured to implement combinatorial logic, including arithmetic operations, as well as for the implementation of automata with memory.

The ALM architecture is compatible with the architecture of the 4-input LUTs, and one ALM can also implement any functions up to six variables and certain functions of seven variables. It is noted that such architecture wins on speed and efficiency (probably, it is a question of hardware expenses and the area of a crystal) – Fig. 1 [4].

In Fig. 1 indicates eight inputs of the adaptive LUT, which may give the impression of the possibility of implementing the 8-LUT. Even more confusing is the information contained in the presentation [9], where it is indicated that for the implementation of $k$-LUT, $2^k$ bits of SRAM and a multiplexer are also needed $2^k$:1, but this is impossible. Different modes of using ALM do not clarify the details (Fig. 2) [4].

Let’s consider the primary source – the documentation on FPGA Stratix III [4], where the details of ALM are shown (Fig. 3).

Thus, it turns out that ALM is built not only on two 4-LUTs, but there are four LUTs in 3 variables (3-LUT), that so, from two 3-LUTs we can get one 4-LUT. Therefore, there are only four 4-LUTs, then it becomes clear how the 6-LUT is constructed – the two older variables $e, f$ choose one of the four. In Fig. 5 control signals are not indicated on a number of multiplexers designated by trapezoids (LUT 1-6 are also multiplexers, but they are shown with control signals, the setting is implied).

3 MATERIALS AND METHODS

Let $k$ be the dimension of the basic LUT ($k \in \{1, 2, 3, 4\}$). For 1-LUT in principle up to $n=4$ there is no need for an output inverter. More than 4 for the indicated restrictions $k$ at the moment is not practiced.

Let’s estimate the complexity of LUT without decomposition (“ideal” complexity, since this can only be up to $n=4$, no more):

$$L_n = 2^n \cdot 8 + 2^{n+1} + 2n,$$

where $2^n \cdot 8$ is the number of tuning elements (six SRAM transistors and two transistors are needed for each input of the tuning to implement the inverter at the input of the transistor tree); $2^n$ – the number of inverters in $n$ variables; $2^{n+1}$ – number of elements of the tree of transmitting transistors with the output inverter.

When decomposing an $n$-tree with $k$ LUT, $k \in \{1, 2, 3, 4\}$, $n \geq k$, $n \leq 8$:

$$L_{nk} = 2^n \cdot 8 + (2^{k+1} + 2k) \cdot 2^{n-k} + (2^{n-k+1} + 2^{n-k+1}) + 2n,$$

where $2^{k+1}$ is the complexity of the tree $k$ LUT; $2^k$ is the number of transistors in $k$ inverters, $2^{n-k}$ need these trees, more LUTs for $2^{n-k}$ inputs (which can also be decomposed) are needed to connect the trees obtained with decomposition of $2^{n-k}$ trees, respectively complexity $2^{n-k+1} + 2 \cdot 2^{n-k} = 2^n + 2^{n-k+1}$, where $2^{n-k+1}$ is the complexity of the tree with the output inverter, $2^2 \cdot 2^{n-k} = 2^{n-k+1}$ – complexity of input inverters. The time delay in the decomposition is estimated by the length of the maximum path in the logical element from the input to the output. At the same time, without decomposition – with the “ideal” version (Figure 2) we get:

$$T_n = n + 2.$$

The path for decomposition in the transmitting transistors is also estimated by the value $n$, but due to additional inverters at the input and output in the LUT chain (Fig. 3, 4), it will be larger:

$$T_{nk} = n + 2 \left[ \frac{n}{k} \right].$$
4 EXPERIMENTS

In the process of investigation, schemes of various variants of the multi-bit LUT ($n > 4$) were obtained and modeled. An example of the synthesis of a 6-LUT of four 4-LUTs and one 2-LUT is shown in Fig. 4.

In Fig. 4 2-LUT inputs have inverters, therefore, since the number of inverters on the signal path is even, the settings are recorded as usual.

5 RESULTS

We restrict ourselves to $n = 8$, so it is assumed that the additional LUT will fit into the required decomposition parameters with $k$ LUT, $k \in \{1, 2, 3, 4\}$. We use the computer mathematics system Mathcad. The graphs for comparing the complexity of the decomposition according to the expression (3) $n$ LUT over $k$ are shown in Fig. 5.

The result is expected – the larger is the building block, the less is the cost for implementing a complex LUT for 5, 6, 7 and 8 variables. The graphs of the change (5) for $n = 5...8$ are shown in Fig. 6.

The graphs of the change (5) for $n = 7...10$ are shown in Fig. 7.

6 DISCUSSION

Thus, in the adaptive logic modules of the Stratix III FPGA there are two 4-LUTs, as indicated in the translation articles. However, in fact there are two more LUTs in 3 variables (3-LUT), from which two additional 4-LUTs can be built. In total, four 4-LUTs are obtained. It is clear how 5-LUT and 6-LUT are built from them. There is no difficulty in obtaining of two 5-LUTs. Therefore, the setting must contain at least 64 bits to specify any function of the six variables. It
is advisable in the future by analyzing the ALM setup to obtain a logical model and check on it the compliance of the declared capabilities of ALM with the variants depicted in the documentation.

CONCLUSIONS

Analyzed decomposition of multi-bit LUT shows, that the most effective in terms of complexity and speed is the use of “building blocks” 4-LUT, as it is indicated in the available sources. It is interesting to build LUT on the basis of so-called 3D transistors, which are already actively used by leading firms. There is information about mitigating the limitations of Meade and Conway in such “advanced” technologies. In addition, it is advisable to investigate the problem of decomposition when introducing the fault tolerance facilities proposed in [10] into the LUT.

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REFERENCES


Figure 4 – 6-LUT, consisting of four 4-LUTs and one 2-LUT
Figure 5 – Comparison of complexity of decomposition $n$ LUT by $k$.

Figure 6 – Comparison of the delay LUT with decomposition for $n=5...8$ by $k$. 


5. Intel HyperFlex FPGA Architecture Overview [electronic resource], access mode: https://www.altera.com/products/fpga/stratix-series/stratix-10/features.html#hyperflexarchitecture


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сделать вывод о дальнейшем увеличении разрядности LUT и сближении возможностей FPGA и CPLD (complex programmable logic devices) в плане разрядности. Поэтому исследования особенностей построения многоразрядных LUT являются актуальными и авторами предпринята попытка анализа реализации такой перспективной многоразрядной логики.

**Цель работы** – оценка сложности и быстродействия при декомпозиции многоразрядного LUT.

**Метод.** Получение выражений для оценок сложности и быстродействия декомпозиции многоразрядного LUT на LUT меньшей разрядности.

**Результаты.** Выполнено сравнение сложности и задержки в количестве транзисторов при декомпозиции многоразрядного LUT в системе компьютерной математики Mathcad.

**Выводы.** Проведенные исследования позволили установить особенности построения многоразрядных LUT и оценивать различные варианты декомпозиции при дальнейшем увеличении разрядности LUT с последующим выбором оптимального варианта ALM.

**Ключевые слова:** логический элемент, ПЛИС типа FPGA, LUT, транзистор, адаптивный логический модуль ALM, декомпозиция, сложность, быстродействие.

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